ABSTRACT OF THE DISCLOSURE

A thin film transistor array substrate includes a gate line assembly and a common line assembly formed on an insulating substrate. The gate line assembly has gate lines proceeding in the horizontal direction, and gate electrodes connected to the gate lines. The common line assembly has a plurality of common electrodes placed within pixel regions, and common signal lines interconnecting the common electrodes. A gate insulating layer covers the gate line assembly and the common line assembly, and semiconductor patterns and light interception patterns are formed on the gate insulating layer with the same material. A data line assembly and a pixel line assembly are formed on the gate insulating layer. The data line assembly has data lines crossing over the gate lines to define the pixel regions, and source/drain electrodes. The pixel line assembly has pixel electrodes proceeding in parallel to the common electrodes while being spaced apart from the common electrodes with a predetermined distance. In order to prevent leakage of light at the periphery of the data lines, each light interception pattern is overlapped with the corresponding data line, and the common or the pixel electrodes positioned close to the data line.